

FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office		Attorney Docket Number 5646-108			Serial No. 10/649,493	
		Applicants: McDonagh et al.				
		Filing Date: August 27, 2003			Group 2817	

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U. S. PATENTS & PATENT APPLICATION PUBLICATIONS							
Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
MB,	1	6,539,072	03-25-03	Donnelly et al.	375	371	
	2	6,125,157	09-26-00	Donnelly et al.	375	371	
	3	5,614,855	03-25-97	Lee et al.	327	158	
mz,	4	5,485,490	5,485,490	Leung et al.	375	371	

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)		
ms	5	Lee et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM," IEEE Journal of Solid-State Circuits, Vol. 29, No. 12, December 1994, pp. 1491-1496

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<b>FORM PTO-1449 U.S. Department of Commerce</b> <b>Patent and Trademark Office</b>  <b>LIST OF DOCUMENTS CITED BY APPLICANT</b>  (Use several sheets if necessary)				Attorney Docket Number 5646-108		Serial No. To Be Assigned  10/649,493	
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